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Title:

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MICROTRANSFORMER FOR SYSTEM-ON-CHIP POWER SUPPLY

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MICROTRANSFORMER FOR SYSTEM-ON-CHIP
POWER SUPPLY

Cross-Reference to Related Application

5   This application is a continuation-in-part of application no.

_____ (U.S. Patent. No. _____), filed December 10, 1999.

Field of the Invention

The present invention relates generally to semiconductor circuits, and

10   in particular to a method for the fabrication of microtransformers which can be

used in a system-on-chip power supply.

Background of the Invention

The system-on-chip concept refers to a system in which, ideally, all

15   the necessary integrated circuits are fabricated on a single die or substrate.

Various packaging schemes have been proposed to achieve integration of chips

with different functionalities in a single package by mounting them on a silicon

interposer to form a circuit module. For example, the simplest scheme is the

chip-on-chip module, in which a microprocessor chip and a memory chip are

20   stacked together, face to face or through a silicon interposer, using micro bump

bonding (MBB) technology.

Integrating all system components into one chip or a plurality of

chips in a single module affords a smaller product size, higher speed, and

increased reliability. Power consumption remains, however, a critical issue,

especially for portable devices having complex circuitry, which requires an always increasing number of devices to be integrated on one chip.

In an effort to reduce the power consumption, power supply components, such as DC-DC converters, intelligent power LSIs, and thin film

5   magnetic devices, have been integrated into one chip. Since a typical DC-DC converter consists of semiconductor devices, resistors, capacitors, and electromagnetic components, such as transformers and inductors, among others, a key issue for the system-on-chip DC-DC converter is integrating both semiconductor and electromagnetic devices into a chip, while reducing the size

10   of the electromagnetic components, which tend to occupy a large amount of space.

For example, U.S. Patent No. 5,279,988 to Saadat and Thomas teaches a processes for fabrication of microcomponents integrated circuits, including microtransformers and microinductors, using multilevel metallization

15   involving six layers of insulators and a coil winding.

U.S. Patent No. 5,583,474 to Mizoguchi et. al. discloses "a planar magnetic element" consisting of a pair of planar spiral coils sandwiched by two thin magnetic films to form an inductor or a transformer.

Similarly, U.S. Patent No. 5,519,582 to Matsuzaki discloses a

20   magnetic induction coil directly mounted on, and integrated with, a semiconductor wafer containing integrated circuitry. Grooves are etched in the reverse face of the wafer substrate, an insulating film is applied, and conducting materials fill the grooves forming therefore the coil.

The implementation of a truly high performance system-on-chip DC-DC converter with electromagnetic elements poses various problems, mainly because of the growing demand for increased efficiency at high frequency operations. High frequency operations are highly desirable for

5   electromagnetic elements since they permit a decrease in the size of the device while affording the same reactance. Yet, at frequencies higher than 1 MHz, operating frequency increases tend to have a detrimental effect on the efficiency of the devices. Multilayered integrated circuit structures for forming electromagnetic components have attempted to address the efficiency issue, but

10   have reached only limited results.

Another disadvantage of electromagnetic devices operating at high frequencies is the limitation posed by the width of the winding conductor. Because the electromagnetic element coil is formed by a thin film conductor, its width must be limited to form the desired fine pitch structure. Consequently,

15   the current capacity of the magnetic induction is also limited and, in turn, limits the current density in the coil.

Further, planar electromagnetic elements fabricated today are not yet small enough to be integrated with other circuit elements, making it practically impossible to manufacture sufficiently small system-on-chip power supplies.

20   There is needed, therefore, a method for further downsizing of electromagnetic elements, for example coils and microtransformers on ICs operating at high frequencies with high efficiency, low losses, and high magnetic permeability. An electromagnetic element for use in a circuit section that will only slightly influence other components of the circuit, will have a sufficiently

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high current capacity and high inductance, and will occupy a minimal substrate area is also needed, as well as a simple process for fabricating such an electromagnetic element.

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Summary of the Invention

The present invention provides an integrated circuit microtransformer capable of operating at high frequencies with high efficiency, low losses, and high magnetic permeability.

The microtransformer of the present invention uses a silicon

10   substrate with a pair of through-holes on which an insulating silicon oxide layer is first deposited on all surfaces of the substrate. A magnetic film, such as Permalloy or others, is further deposited on the silicon oxide layer followed by the application of another insulating layer. Coils are fabricated next by patterned deposition on both sides of the substrate and through the holes. The

15   pair of through-holes allows the winding of a single coil or the winding of primary and secondary coils to pass through the holes and thus to reside on both surfaces of the substrate. The typical through-hole size is approximately 1mm, which can accommodate, for example, up to 83 windings of 8 μm lines on a 12 μm spacing. The coils can be, for example, single coils, or primary or

20   secondary coils of a transformer structure, with secondary coils having one or more output taps to supply different output voltages. For better flux closure, various magnetic layers and insulators can be deposited on top of the windings. The primary and secondary windings of a transformer can also be wound through the holes, but at different levels.

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Advantages and features of the present invention will become more readily apparent from the following detailed description of the invention, which is provided in connection with the accompanying drawings.

Brief Description of the Drawings

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Fig. 1 is a schematic diagram of a conventional DC-DC converter.

Fig. 2 illustrates a one-chip power supply DC-DC converter

10   incorporating a microtransformer of the present invention.

Figs. 3-5 show a portion of a silicon substrate undertaking a sequence of steps for through-hole fabrication, performed in accordance with a method of forming a microtransformer of the present invention.

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Fig. 6 is top view of a representative substrate of the present invention with the through-holes fabricated therein.

Fig. 7 is a bottom view of a representative substrate of the present

20   invention with the through-holes fabricated therein.

Fig. 8 is a cross-sectional view of the representative microtransformer of Fig. 6, taken along line 8-8', at an intermediate stage of processing and in accordance with a first embodiment of the present invention.

Fig. 9 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing subsequent to that shown in Fig. 8.

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Fig. 10 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing subsequent to that shown in Fig. 9.

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Fig. 11 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing subsequent to that shown in Fig. 10.

Fig. 12 is a cross-sectional view of the representative

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microtransformer according to the present invention at a stage of processing subsequent to that shown in Fig. 11.

Fig. 13 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing

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subsequent to that shown in Fig. 12.

Fig. 14 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing subsequent to that shown in Fig. 13, illustrating a fabricated coil structure.

Fig. 15 is a cross-sectional view similar to that of Figs. 3-5, showing a fabricated coil structure of the representative microtransformer in accordance with the first embodiment of the present invention.

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Fig. 16 is a is a cross-sectional view of the representative microtransformer of Fig. 6, taken along line 16-16' and in accordance with the first embodiment of the present invention.

10 Fig. 17 is a top view of the representative microtransformer of the first embodiment of the present invention with fabricated coil structure formed on both sides of the substrate and through the holes.

Fig. 18 is a cross-sectional view of the representative

15 microtransformer according to a first embodiment of the present invention at a stage of processing subsequent to that shown in Fig. 14.

Fig. 19 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing

20 subsequent to that shown in Fig. 14 and in accordance with a second embodiment of the invention.

Fig. 20 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing subsequent to that shown in Fig. 19.

5   Fig. 21 is a cross-sectional view of the representative microtransformer according to the present invention at a stage of processing subsequent to that shown in Fig. 19 and in accordance with a third embodiment of the present invention.

10   Fig. 22 is a cross-sectional view similar to that of Figs. 3-5 showing two layers of a fabricated coil structure of the representative transformer of the present invention and in accordance with a third embodiment.

Fig. 23 is a cross-sectional view of an integrated circuit package
15   containing the representative microtransformer of the present invention electrically connected to a die.

Fig. 24 is a schematic diagram of a processor system incorporating a microtransformer of the present invention.

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Detailed Description of the Preferred Embodiments

In the following detailed description, reference is made to various exemplary embodiments for carrying out the invention. These embodiments

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are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural, electrical and process changes may be made, and equivalents substituted, without departing from the invention. Accordingly, the

5   following detailed description is exemplary and the scope of the present invention is defined by the appended claims.

The term "substrate" used in the following description includes any semiconductor-based structure having an exposed silicon surface in which the structure of this invention may be formed. The term "substrate" is to be

10   understood as including substrates formed of silicon, silicon-on-insulator, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a substrate in the following description, previous process steps may have been utilized to form regions or junctions in, or material

15   layers on, the base semiconductor structure or foundation.

Referring now to the drawings, where like elements are designated by like reference numerals, Fig. 1 illustrates a circuit diagram of a single-ended forward DC-DC converter 10, which is a key component for a power supply. The DC-DC converter 10 comprises a voltage source 8, a microtransformer 14,

20   a switch transistor 20, a control circuit 16 for switch-operating transistor 20 on and off, a rectifier 22, an R/C filter 6, and a load circuit 18. The DC-DC converter 10 can be used to step up or down a DC input voltage V. The output voltage of microtransformer 14 is rectified by diode rectifiers 22 and smoothed by R/C circuit 6 to supply an output DC voltage to load circuit 18.

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Fig. 2 further schematically illustrates a top view the power supply DC-DC converter 10 integrated on a single semiconductor substrate 40. With microtransformer 14 integrated on the same substrate as the other components, the one-chip DC-DC converter 10 has increased reliability and can attain a

5   higher operating frequency with a reduction in the size of the power supply because of a reduced number of parts and shorter wire bonding length. Substrate 40 may also have other digital or analog circuitry integrated thereon, including, for example, logic, processor, and/or memory circuits.

The fabrication of the components of power supply DC-DC

10   converter 10 on substrate 40, save transformer 14, is accomplished by using well-known integrated circuit fabrication techniques. The fabrication of transformer 14 will be discussed greater in detail below.

Figs. 3-5 illustrate a sequence of steps for forming a pair of through-holes 43, 45, in the substrate 40 in the area where transformer 14 will be

15   fabricated. This is the first step in the fabrication of transformer 14. Precise details of one through-hole fabrication technique that can be employed were given recently by Christensen et al., in *Wafer Through-Hole Interconnections with High Vertical Wiring Densities*, IEEE Trans. on Components, Packaging and Manufacturing Technology, Pt. A, vol. 19, no. 4, 516-22 (1996), the

20   disclosure of which is incorporated by reference herein, and will not be repeated in detail here. A brief summary of these steps is believed helpful to attain a better understanding of the subsequent fabrication steps.

The through-hole fabrication is an anisotropic etching into an oriented silicon substrate with rectangular openings in the etch mask on one

side of the wafer along the lattice planes. The definition of a pair of holes in the

silicon substrate 40 of Fig. 3 begins by forming an etch mask of a thermally

grown oxide 42 on both sides of the silicon substrate 40. As shown in Fig. 3,

the mask 42 on one side of the substrate 40 is patterned to have the rectangular

5   openings therein.

Next, as shown in Fig. 4, the masking layer 42 with rectangular mask

openings is used to anisotropically etch the substrate 40 from one surface of

substrate 40 towards the other surface of substrate 40 and through the bottom

oxide layer 42 in an aqueous etching solution, so that holes 43 and 45 are

10   formed. The side wall of each hole is at a 54.7° angle, α, that is defined by the

openings in the masking layer 42 and lattice plane 111 of the substrate 40. The

typical hole size is approximately 1mm square at the upper surface of the

substrate 40.

Next, as shown in Fig. 5, a thick thermal oxide 44 is grown over all

15   exposed areas of the substrate, including the side walls defining holes 43, 45.

This layer acts as an insulating layer between the substrate and subsequent

formed layers, and it also rounds the sharp corners at the top and bottom of the

through-holes 43 and 45.

Fig. 6 shows a top view of the substrate 40 with the holes 43, 45

20   formed therein and with the fabricated oxide layer 44. Fig. 7 represents a

bottom view of the substrate 40 with the through-holes 43, 45 formed therein

and the oxide layer 44.

Oxide layer 44 can be formed over the entire top and bottom

surfaces of the substrate 40 and then etched to only remain on these surfaces in

the area between holes 43 and 45 and on the side walls shown as CDGH and ABEF in Fig. 6. Alternatively, oxide layer 44 can be left to cover the entirety of the top and bottom surfaces of substrate 40, depending on other processing steps which may be utilized to create other structures in substrate 40.

5   Once the through-holes 43 and 45 are formed and the oxide layer 44 grown, the next step is the fabrication of a transformer core 50 on silicon substrate 40 in the area between holes 43, 45. This area is illustrated in Fig. 6 as the area bounded by letters A, B, C and D on the top surface of the substrate; the area of the side wall of hole 43 bounded by the letters C, D, G and H; the

10   area of the side wall of the hole 45 bounded by the letters A, B, E and F; and the area on the lower surface of the substrate 40 bounded by the letters E, F, G and H, as shown in Fig. 7.

In our exemplary embodiment, substrate 40 is a silicon substrate of <100> crystal orientation. It can be undoped in the area in which transformer

15   14 will be formed, or it can be doped to either a p or n conductivity as necessary or convenient for forming devices in other portions of substrate 40.

Referring now to Fig. 8, which is a partial cross-sectional view along the line 8-8' in Fig. 6, oxide layer 44 is preferably an oxide, such as a thermal oxide of silicon, or a nitride. Oxide layer 44 is approximately 1 μm thick and is

20   a first insulating layer, which also acts as a substrate passivation layer. A high temperature polymer film such as a polyimide can also be used in place of oxide layer 44. For example, a polyimide with a low dielectric constant (ε=3) may be deposited by spin coating followed by curing, if required by electrical design.

Reference is now made to Fig. 9. Subsequent to the formation of oxide layer 44, either a dry process or a wet process may be employed for the deposition of a soft magnetic film structure 70 on top of insulating layer 44. The total thickness of the soft magnetic film structure 70 of Fig. 9 is between

5   about 2 to about 4 μm.

The magnetic material for the soft magnetic layer 70 may be one of the following choices: (1) magnetic films laminated with insulating spacers, such as Permalloy (NiFe), NiFeMo, Co-Zr, CoZrRe, CoFeSiB, CoNbZr, and Co-Cr-O granular films; or (2) a magnetic film laminated with another

10   magnetic film, such as Fe –X –N alloy or Fe –X—B—N alloy where X is at least one atom selected from the group consisting of Zr, Hf, Ti, Nb, Ta, V, Mo, W, and Cr. For example, Fe/FeN, FeCoV/FeNiMo, FeN/AlN, CoBN/AlN, and FeAl/FeN are only few of the choices for the material of the magnetic layer 70. Ultimately, the choice depends upon the deposition requirements of the

15   magnetic material and upon the further processing requirements such as post deposition annealing and patterning. Ni-Fe or other Permalloy materials which can be easily formed through sputtering are preferred, although other materials with analogous properties may work as well.

Referring now to Fig. 10, a second insulating layer 62 is deposited

20   over magnetic layer 70. The second insulating layer 62 provides electrical isolation for the winding wires. It must be noted that insulating layers, such as layer 62, are necessary for the isolation of the winding wires only when the magnetic material of the soft magnetic layers, such as layer 70, is a conductive magnetic material, such as Ni-Fe alloy or a ferromagnetic material. When,

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however, the magnetic material of the soft magnetic layers is an insulating

magnetic material, such as an iron oxide, for example, insulating layers, such as

layer 62, that isolate the winding wires from the magnetic layers are not

necessary.

5   Any standard IC technique for fabricating the insulating layer 62 can

be employed, such as simple evaporation or sputtering. For example SiO_2 or

Si_3N_4 may be deposited by CVD to a thickness of 0.5 to 1 μm. A high

temperature polymer film such as a polyimide may be employed also.

Next, the coil windings are formed. Standard IC technology for the

10   fabrication of primary and secondary coil windings involves optical lithography

and deposition of high-conductivity metals such as copper or silver with a fine

pitch. Either a dry process, such as evaporation or sputtering of a metal film

followed by dry etching, or a wet process, such as electrochemical plating to

form the individuals conductors, could be employed. In both cases, typical

15   width and height of the coil winding is 8 μm each with spacing of 4 μm

between primary and secondary windings.

Reference is now made to Fig. 11, which illustrates the beginning of

the deposition of coil winding structure 100 (Fig. 14) by a dry process, such as

sputtering. The first step under this dry process, as shown in Fig. 11, is the

20   formation of a conductive material layer 80 over the second insulating layer 62,

which in turn covers magnetic layer 70. The conductive material layer 80 is

formed of copper (Cu), or other suitable conductive material, having a thickness

of approximately 10 μm.

As illustrated in Fig. 12, as part of the patterning of conductive material layer 80, a photoresist film 82 is then coated on the conductive copper layer 80. A UV mask (not shown) is placed over the photoresist film 82, which has the conductor pattern therein for forming a coil layer. As in any

5 conventional photolithography process, the mask has areas which allow UV light to pass through and contact the photoresist layer 82. The mask also includes areas that block the UV light from contacting the photoresist layer 82. The UV light contacts the photoresist mask layer 82 and develops it so that developed photoresist areas 84 are left as shown in Fig. 13.

10 The underlying conductive material layer 80 is next etched through the developed photoresist film 82. Etching can be done with a plasma etch and then the remaining photoresist film areas 84 are removed with subsequent processing. The resultant coil structure 100 is illustrated in Fig. 14. The coil structure 100 which is formed contains both primary, such as 104, and

15 secondary, such as 108, coils of microtransformer 14 with their windings interleaved. Alternatively, if desired, the conductive material layer 80 can be etched to form only a single continuous coil.

A cross-sectional view of the silicon structure 40 of Fig. 14, taken along the line 16-16' shown in Fig. 6, after fabrication of the coil structure 100,

20 is shown in Fig. 16. The inclination of coil winding is defined by angle δ. A side view of the microtransformer 14 with the fabricated coil structure 100 formed on both sides of the substrate 40 and through the holes 43 and 45 is illustrated in Fig. 15. A top view is shown in Fig. 17.

Deposition is not the only method that could be employed for forming the conductive material layer 80. The conductive material layer 80 can be also electroplated over insulating layer 62. Under this wet process and using copper as the conductive material, a thick copper layer may be electroplated on

5   top of a thin, vacuum-evaporated (sputtered) base metal (i.e. base copper) having a thickness of approximately 1000Å. The base metal adheres to a suitable bonding layer that is formed directly on the substrate insulating material. The bonding layer may be composed of bonding materials such as titanium (Ti), titanium-tungsten (Ti/W) or chromium, among others. The role

10   of the bonding layer is to form a strong mechanical and chemical bond between the copper conductor and the underlying substrate to help prevent peeling of the formed conductive layer off the substrate. After the conductive layer 80 is electroplated on insulating layer 62, it can be etched in the manner described above to form the coil structure 100.

15   As known in the art, increasing the number of coil windings will increase the electrical resistance of the coil. Thus, to reduce the electrical resistance, it is desirable to employ coils with larger cross section that are fabricated with a low-resistivity conductor such as copper. Of these, copper windings with an aspect ratio of at least one or higher are recommended. For

20   example, the copper coils could have 8μm in width and height each, with a spacing of 4μm between the primary and the secondary windings.

Following coil formation, a top protective insulating layer 63 is next deposited over the coil structure 100 as shown in Fig. 18. A passivating layer 65 can be also deposited on top of top protective insulating layer 63. Vias can

be provided as needed to interconnect microtransformer 14 with other structures of DC-DC converter 10, which are integrated elsewhere in substrate 40.

In another embodiment, and in order to increase the flux coupling between the primary and the secondary coils, another magnetic layer 72 can be applied on top of the coil winding structure 100 before the final top protective insulating layer 63 or passivating layer 65 are applied. This is shown in Fig. 19. First, a second insulating layer 64 is applied over the coil structure 100 and then another magnetic layer 72 is applied. Any standard IC processing technique, such as simple evaporation, sputtering, or electroplating, may be used to deposit insulating layer 64. For example SiO_2 or Si_3N_4 may be deposited by CVD to a thickness of 0.5 to 1 μm.

Layer 72 can now be formed over layer 64 in the same manner and to the same thickness as layer 70. The same types of materials as employed for layer 70 can also be used for layer 72. Layer 72 may then be covered by another top protective insulating layer 67 and a passivating layer 69 to complete the transformer structure, as illustrated in Fig. 20. In both the Fig. 18 and Fig. 20 structures, the final top protective insulating and passivating layers (63, 65 in Fig 18) (67, 69 in Fig. 20) can be formed as a single layer, the two layers shown, or as three or more layers of top protective insulating and/or passivating layers.

According to another embodiment of the present invention, to further improve the magnetic flux coupling, a second coil winding structure 112

can be deposited on top of the first coil winding structure 100 using the same techniques as used to form coil winding structure 100. In this embodiment, which is illustrated in Figs. 21-22, the first coil winding structure 100 can be one of the primary and secondary windings of the microtransformer 14, while

5   the secondary coil winding structure 112 can be used as the other of the primary and secondary winding. The second winding layer 112 may be provided with several output taps to provide output voltages.

The IC mictrotransformer 14 provided by the present invention is capable of operating at high frequencies, with high efficiency, low losses, and

10   high magnetic permeability. The coil winding structure (100 in Figs. 14-20; 100, 112 in Fig. 21) of mictrotransformer 14 further allows for a reduction in the overall size while retaining an optimal geometry for the production of high quality (Q) factors. A Q factor is dependent upon resistance and inductance. In the industry, maximizing Q has proven difficult mainly because of the

15   necessary limitations set by theoretically effective integrated systems (i.e. size, power, etc.). Thus, using the through-holes in a semiconductor substrate for winding the primary and the secondary windings, the coil winding structure 100 increases the magnetic flux coupling and the inductance, which in turn affords a higher Q factor.

20   The material for the substrate 40 is not limited as long as the four surfaces at issue are electrically insulated to prevent undesired electrical shortings. For example, other substrates such as quartz, Al_2O_3/TiC, ceramics, ferromagnetic materials, and semiconductor material other than silicon are also appropriate substrate materials. Nevertheless, to promote the readiness for

micro processing and facilitate the production of a one-chip device, it is desirable that the substrate 40 be formed of a semiconductor material.

Although the drawings show a relatively thin substrate 40 in comparison to the thickness of the insulating layers 62, 63, 64, 65, 67 or 68 in actuality these insulating layers are thin in comparison to the substrate 40. However, having a thickness of approximately 1 to 2 µm, these insulating layers are approximately twice, or more, as thick as oxide layers normally employed in IC processes. Further, as mentioned above, insulating layers, such as layers 62, 64 or 68, may be necessary or not depending on whether the magnetic material for the magnetic layers, which contact the coil winding 100 or 112, is a conducting or an insulating magnetic material.

The insulating material used for the insulating layers mentioned above is preferably an inorganic compound such as silicon oxide (for example SiO_2 produced by sputtering or CVD or PECVD, and SiO by evaporation) or silicon nitride. Organic compounds may be used also. For example, a high-temperature polyimide from Du Pont may be used for the insulating layers if the subsequent processes are not subjected to a high temperature processing.

The primary and secondary coil conductors of microtransformer 14 are made of low-resistivity metal. Although copper (Cu) has been described above as exemplary, any low resistivity metal can be used including aluminum (Al), Al-alloys, gold (Au), Au-alloys, silver (Ag), or Ag-alloys. An alloy of copper, such as Al-Cu alloy, may be used also. Materials for coil conductors, however, are not limited to these examples. The rated current of the coil winding structure 100 is proportional to the permissible current density of the

low-resistivity material of the conductors. Hence, it is desirable that the material be one that is highly resistant to electromigration, stress migration, or thermal migration.

A high performance system-on-chip may be provided by integrating the other components of the DC-DC converter and load circuits in, or on, other areas of substrate 40 as shown in Fig. 2. Alternatively, substrate 40 can be used as an interposer for mounting other IC chips to it, since it contains the fabricated transformer 14 and the other components of the DC-DC converter, using, for example, MBB bonding technology as is known in the art to produce a chip-on-chip system.

Fig. 23 illustrates the interconnection between the substrate 40, containing fabricated microtransformer 14, and a die 13, which together produce a complete IC package 11. Bonding sites 23 are defined on substrate 40. During packaging, an electrical connection is formed between the die 13 and substrate 40 by placing the die 13 onto the substrate 40 so that bonding sites 23 come into contact with electrical interconnect structures 25, such as solder balls, to thereby electrically and mechanically connect together die 13 and substrate 40.

Fig. 24 is a block diagram of a processor-based system 200 utilizing RAM 212 memory, which contains at least one integrated circuit having a DC-DC converter constructed in accordance with the present invention. That is, the RAM 212 employs a DC-DC converter containing the microtransformer 14 of the invention. The processor-based system 200 may be a computer system, a

process control system, or any other system employing a processor and associated memory.

The system 200 includes a central processing unit (CPU) 202, for example, a microprocessor, that communicates with the RAM 212 and an I/O device 208 over a bus 220. It must be noted that the bus 220 may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus 220 has been illustrated as a single bus.

A second I/O device 210 is illustrated but is not necessary to practice the invention. The processor-based system 200 also includes read-only memory (ROM) 214 and may include peripheral devices such as a floppy disk drive 204 and a compact disk (CD) ROM drive 206, which also communicate with the CPU 202 over the bus 220, as is well known in the art.

The above description and drawings illustrate preferred embodiments that achieve the features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments, as many modifications and substitutions can be made without departing from the spirit and scope of the invention. Any modification of the present invention that comes within the scope of the following claims should be considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is: